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CMOS Time Characteristics Formulas

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List of 17 CMOS Time Characteristics Formulas

CMOS Time Characteristics

1) Acceptable MTBF

$$\text{fx } \text{MTBF} = \frac{1}{P_{\text{fail}}}$$

[Open Calculator !\[\]\(a870788d6ed9b8fd294b7654a8c8526b_img.jpg\)](#)

$$\text{ex } 2.5 = \frac{1}{0.4}$$

2) Aperture Time for Falling Input

$$\text{fx } t_{\text{af}} = T_{\text{setup0}} + T_{\text{hold1}}$$

[Open Calculator !\[\]\(c50c8b7b2cc2cf9ff925edec0ee94c0d_img.jpg\)](#)

$$\text{ex } 11.65\text{ns} = 3.75\text{ns} + 7.9\text{ns}$$

3) Aperture Time for Rising Input

$$\text{fx } t_{\text{ar}} = T_{\text{setup1}} + T_{\text{hold0}}$$

[Open Calculator !\[\]\(f60b7a900783ac3fd531bfd9c111be6d_img.jpg\)](#)

$$\text{ex } 14\text{ns} = 5\text{ns} + 9\text{ns}$$

4) Hold Time at High logic

$$\text{fx } T_{\text{hold1}} = t_{\text{af}} - T_{\text{setup0}}$$

[Open Calculator !\[\]\(83bbbd261710c59db0214aa27b2edc0d_img.jpg\)](#)

$$\text{ex } 7.9\text{ns} = 11.65\text{ns} - 3.75\text{ns}$$



5) Hold Time at Low logic

$$fx \quad T_{hold0} = t_{ar} - T_{setup1}$$

[Open Calculator !\[\]\(cbe80b694ebd74fcfe136a095b608235_img.jpg\)](#)

$$ex \quad 9ns = 14ns - 5ns$$

6) Initial Voltage of Node A

$$fx \quad A_0 = V_m + a_0$$

[Open Calculator !\[\]\(3e2231b1ad3ca8da8658228c00dd08e0_img.jpg\)](#)

$$ex \quad 18V = 8V + 10V$$

7) Metastable Voltage

$$fx \quad V_m = A_0 - a_0$$

[Open Calculator !\[\]\(0d5ec72f61334709c3fc9450209b754f_img.jpg\)](#)

$$ex \quad 8V = 18V - 10V$$

8) Phase Detector Average Voltage

$$fx \quad K_{pd} = \frac{i_{pd}}{\Phi_{err}}$$

[Open Calculator !\[\]\(b64b40baaee5acddc1eab8538ba84754_img.jpg\)](#)

$$ex \quad 3.079987V = \frac{499.93mA}{9.30^\circ}$$


9) Probability of Synchronizer Failure

$$fx \quad P_{fail} = \frac{1}{MTBF}$$

[Open Calculator !\[\]\(aff7c69c44a5e015f18c35867ef3f5c3_img.jpg\)](#)

$$ex \quad 0.4 = \frac{1}{2.5}$$




10) Setup Time at High Logic 

$$fx \quad T_{\text{setup1}} = t_{\text{ar}} - T_{\text{hold0}}$$

[Open Calculator !\[\]\(e78f798d4ea5c530c9db49e7d26e6b95_img.jpg\)](#)


$$ex \quad 5\text{ns} = 14\text{ns} - 9\text{ns}$$

11) Setup Time at Low Logic 

$$fx \quad T_{\text{setup0}} = t_{\text{af}} - T_{\text{hold1}}$$

[Open Calculator !\[\]\(05be7c7a8995decd503647c99211f7c2_img.jpg\)](#)

$$ex \quad 3.75\text{ns} = 11.65\text{ns} - 7.9\text{ns}$$

12) Small Signal Offset Voltage 

$$fx \quad a_0 = A_0 - V_m$$

[Open Calculator !\[\]\(fe3aebe81acea8d45108cd2768939da7_img.jpg\)](#)

$$ex \quad 10\text{V} = 18\text{V} - 8\text{V}$$

13) XOR Phase Detector Current 

$$fx \quad i_{\text{pd}} = \Phi_{\text{err}} \cdot K_{\text{pd}}$$

[Open Calculator !\[\]\(899d8b7697d64725bf017d3296cfcf1b_img.jpg\)](#)

$$ex \quad 499.9321\text{mA} = 9.30^\circ \cdot 3.08\text{V}$$

14) XOR Phase Detector Phase 

$$fx \quad \Phi_{\text{err}} = \frac{V_{\text{pd}}}{K_{\text{pd}}}$$

[Open Calculator !\[\]\(40770d9ed6ed4f1222ebf89a1396e8b2_img.jpg\)](#)

$$ex \quad 9.301263^\circ = \frac{0.50\text{V}}{3.08\text{V}}$$



15) XOR Phase Detector Phase with reference to Detector Current 

$$fx \quad \Phi_{err} = \frac{i_{pd}}{K_{pd}}$$

[Open Calculator !\[\]\(e2376d476d06eb31946dc01a69a4403a_img.jpg\)](#)

$$ex \quad 9.299961^\circ = \frac{499.93mA}{3.08V}$$

16) XOR Phase Detector Voltage 

$$fx \quad V_{pd} = \Phi_{err} \cdot K_{pd}$$

[Open Calculator !\[\]\(0b5e7e25e8775f7e7e80906ada4f0021_img.jpg\)](#)

$$ex \quad 0.499932V = 9.30^\circ \cdot 3.08V$$

17) XOR Voltage NAND Gate 

$$fx \quad V_x = \frac{C_y \cdot V_{bc}}{C_x + C_y}$$

[Open Calculator !\[\]\(bd3b31712ad9bab5a241210fa6925cdd_img.jpg\)](#)

$$ex \quad 0.881972V = \frac{3.1mF \cdot 2.02V}{4mF + 3.1mF}$$








Variables Used

- a_0 Small Signal Offset Voltage (Volt)
- A_0 Initial Node Voltage (Volt)
- C_x Capacitance 1 (Millifarad)
- C_y Capacitance 2 (Millifarad)
- i_{pd} XOR Phase Detector Current (Milliampere)
- K_{pd} XOR Phase Detector Average Voltage (Volt)
- **MTBF** Acceptable MTBF
- P_{fail} Probability of Synchronizer Failure
- t_{af} Aperture Time for Falling Input (Nanosecond)
- t_{ar} Aperture Time for Rising Input (Nanosecond)
- T_{hold0} Hold Time at Low Logic (Nanosecond)
- T_{hold1} Hold Time at High Logic (Nanosecond)
- T_{setup0} Setup Time at Low Logic (Nanosecond)
- T_{setup1} Setup Time at High Logic (Nanosecond)
- V_{bc} Base Collector Voltage (Volt)
- V_m Metastable Voltage (Volt)
- V_{pd} XOR Phase Detector Voltage (Volt)
- V_x XOR Voltage Nand Gate (Volt)
- Φ_{err} XOR Phase Detector Phase (Degree)



Constants, Functions, Measurements used

- **Measurement: Time** in Nanosecond (ns)
Time Unit Conversion 
- **Measurement: Electric Current** in Milliampere (mA)
Electric Current Unit Conversion 
- **Measurement: Angle** in Degree (°)
Angle Unit Conversion 
- **Measurement: Capacitance** in Millifarad (mF)
Capacitance Unit Conversion 
- **Measurement: Electric Potential** in Volt (V)
Electric Potential Unit Conversion 



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- **CMOS Design Characteristics Formulas** 
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