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CMOS Delay Characteristics Formulas

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List of 13 CMOS Delay Characteristics Formulas

CMOS Delay Characteristics

1) Delay of 1-Bit Propagate Gates

Open Calculator

fx $$t_{pd} = T_{delay} - ((N_{gates} - 1) \cdot t_{AO} + t_{XOR})$$

ex $$70.9\text{ns} = 300\text{ns} - ((10 - 1) \cdot 21.9\text{ns} + 32\text{ns})$$

2) Delay of AND-OR Gate in Gray Cell

Open Calculator

fx $$t_{AO} = \frac{T_{delay} - t_{pd} - t_{XOR}}{N_{gates} - 1}$$

ex $$21.88889\text{ns} = \frac{300\text{ns} - 71\text{ns} - 32\text{ns}}{10 - 1}$$

3) Delay Rise

Open Calculator

fx $$T_d = t_{ir} + (R_{rise} \cdot C_d) + (t_{sr} \cdot t_{prev})$$

ex $$98.484\text{ns} = 2.1\text{ns} + (7.68\text{m}\Omega \cdot 12.55\mu\text{F}) + (100\text{ns} \cdot 5.6\text{ns})$$

4) Edge Rate

Open Calculator

fx $t_e = \frac{t_r + t_f}{2}$

ex $6\text{ns} = \frac{2.8\text{ns} + 9.2\text{ns}}{2}$

5) Fall Time

Open Calculator

fx $t_f = 2 \cdot t_e - t_r$

ex $9.2\text{ns} = 2 \cdot 6\text{ns} - 2.8\text{ns}$

6) Normalized Delay

Open Calculator

fx $d = \frac{t_{pd}}{t_c}$

ex $221.1838 = \frac{71\text{ns}}{0.321\text{ns}}$

7) Propagation Delay

Open Calculator

fx $t_{pd} = d \cdot t_c$

ex $70.99878\text{ns} = 221.18 \cdot 0.321\text{ns}$

8) Propagation Delay in Circuit

Open Calculator

fx $$t_{ckt} = \frac{t_{pHL} + t_{pLH}}{2}$$

ex $$8.16ns = \frac{7ns + 9.32ns}{2}$$

9) Propagation Delay without Parasitic Capacitance

Open Calculator

fx $$t_c = \frac{t_{ckt}}{d}$$

ex $$0.036893ns = \frac{8.16ns}{221.18}$$

10) Rise Time

Open Calculator

fx $$t_r = 2 \cdot t_e - t_f$$

ex $$2.8ns = 2 \cdot 6ns - 9.2ns$$

11) Small Deviation Delay

Open Calculator

fx $$\Delta T_{out} = K_{vcdl} \cdot \Delta V_{ctrl}$$

ex $$8 = 4 \cdot 2V$$

12) VCDL Gain

Open Calculator

fx $$K_{vcdl} = \frac{\Delta T_{out}}{\Delta V_{ctrl}}$$

ex $$4 = \frac{8}{2V}$$

13) Voltage-Controlled Delay Line

Open Calculator

fx $$\Delta V_{ctrl} = \frac{\Delta T_{out}}{K_{vcdl}}$$

ex $$2V = \frac{8}{4}$$

Variables Used

- C_d Delay Capacitance *(Microfarad)*
- d Normalized Delay
- K_{vcdl} VCDL Gain
- N_{gates} Gates on Critical Path
- R_{rise} Rise Resistance *(Milliohm)*
- t_{AO} Delay of AND OR Gate *(Nanosecond)*
- t_c Propagation Delay Capaitance *(Nanosecond)*
- t_{ckt} Circuit Propagation Delay *(Nanosecond)*
- T_d Delay Rise *(Nanosecond)*
- T_{delay} Critical Path Delay *(Nanosecond)*
- t_e Edge Rate *(Nanosecond)*
- t_f Fall Time *(Nanosecond)*
- t_{ir} Intrinsic Rise Delay *(Nanosecond)*
- t_{pd} Total Propagation Delay *(Nanosecond)*
- t_{pHL} Propagation Delay High to Low *(Nanosecond)*
- t_{pLH} Propagation Delay Low to High *(Nanosecond)*
- t_{prev} Delay Previous *(Nanosecond)*
- t_r Rise Time *(Nanosecond)*
- t_{sr} Slope Rise *(Nanosecond)*
- t_{XOR} XOR Gate Delay *(Nanosecond)*

- ΔT_{out} Small Deviation Delay
- ΔV_{ctrl} Voltage-Controlled Delay Line *(Volt)*

Constants, Functions, Measurements used

- Measurement: **Time** in Nanosecond (ns)
  Time Unit Conversion
- Measurement: **Capacitance** in Microfarad (µF)
  Capacitance Unit Conversion
- Measurement: **Electric Resistance** in Milliohm (mΩ)
  Electric Resistance Unit Conversion
- Measurement: **Electric Potential** in Volt (V)
  Electric Potential Unit Conversion

Check other formula lists

- Array Datapath Subsystem Formulas
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